12. (Amended) A stacked gate region of a nonvolatile memory cell having a NOR structure comprising:

a substrate having at least one semiconductor layer;

at least one sloped trench formed in said substrate, said at least one sloped trench having a base and an opening wider than said base;

field oxide deposited in said at least one sloped trench and extending above an upper surface of said substrate;

a tunnel oxide layer formed over at least a portion of said substrate;

at least one floating gate layer formed over said tunnel oxide layer; and

at least one polysilicon ear formed on said at least one floating gate layer and adjacent to said field oxide.

19. (Amended) A stacked gate region of a nonvolatile memory cell having a NOR structure comprising:

a substrate having at least one semiconductor layer;

a plurality of sloped trenches formed in said substrate, said sloped trenches each having a base and an opening wider than said base;

respective field oxide regions formed in said sloped trenches;

a tunnel oxide layer formed over said substrate;

a floating gate layer formed over said tunnel oxide layer; and

a pair of polysilicon ears formed adjacent to corresponding ones of said field oxide regions on said floating gate layer and projecting substantially perpendicular to an upper surface of the floating gate layer.

20. (Amended) The stacked gate region of claim 19, wherein the floating gate layer comprises a plurality of floating gates and a corresponding pair of polysilicon ears for each of the plurality of floating gates.

21. (Amended) A stacked gate region of a nonvolatile memory cell having a NOR structure comprising:

a substrate having at least one semiconductor layer;

a plurality of sloped trenches formed in said substrate, said sloped trenches each having a base and an opening wider than said base;

respective field oxide regions formed in said sloped trenches;

a tunnel oxide layer formed over said substrate;

a floating gate layer formed over said tunnel oxide layer; and

a pair of polysilicon ears adjacent to a portion of said floating gate layer.

22. (Amended) The stacked gate region of claim 21, wherein the floating gate layer comprises a plurality of floating gates and a corresponding pair of polysilicon ears for each of the plurality of floating gates.

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24. (Amended) A nonvolatile memory cell having a NOR structure comprising:

a substrate having at least one semiconductor layer;

at least one sloped trench formed in said substrate, said at least one sloped trench having a base and an opening wider than said base;

a drain formed in said substrate;

a source formed in said substrate;

field oxide deposited in said at least one sloped trench and extending above an upper surface of said substrate;

a tunnel oxide layer formed over at least a portion of said substrate;

at least one floating gate layer formed over said tunnel oxide layer;

at least one polysilicon ear formed on said at least one floating gate layer and adjacent to said field oxide;

a dielectric layer formed over said substrate and said floating gate layer; and

a control gate layer formed over said dielectric layer.

25. (Amended) A nonvolatile memory cell having a NOR structure comprising:

a substrate having at least one semiconductor layer;

at least one sloped trench formed in said substrate, said at least one sloped trench having a base and an opening wider than said base;

a drain formed in said substrate;

a source formed in said substrate;

a tunnel oxide layer formed over at least a portion of said substrate;

at least one floating gate layer formed over said oxide layer;

field oxide deposited in said at least one sloped trench;

at least one polysilicon ear formed on said at least one floating gate layer;

a dielectric layer formed over said substrate and said floating gate layer; and

a control gate layer formed over said dielectric layer.

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33. A nonvolatile memory device having a NOR structure comprising:

a source formed in a substrate;

a drain formed in the substrate;

a floating gate formed over the substrate;

a field oxide deposited in at least one sloped trench formed in the substrate, said at least one sloped trench having a base and an opening wider than said base; and

an ear formed over the substrate.

34. The memory device of claim 33, wherein the ear is comprised of polysilicon.

36. The memory device of claim 33, wherein the ear extends substantially beyond bounds of the floating gate.

37. (Amended) The memory device of claim 33, wherein near vertical sides of the ear do not contact the floating gate.

38. (Amended) The memory device of claim 33, wherein a near vertical edge the ear is adjacent the field oxide and a bottom edge of the ear is adjacent the floating gate.

40. (Amended) A nonvolatile memory device having a NOR structure comprising:

a plurality of memory cells having a plurality of rows, each memory cell comprising:

a control gate, associated with a row, formed integral to a common word line associated with the row,

a source formed in a common region with a source of an adjacent memory cell,

a drain formed in another common region with a drain of an adjacent memory cell,

a floating gate deposited in at least one sloped trench formed in the common region between the source and the drain, said at least one sloped trench having a base and an opening wider than said base, and

a pair of ears;

a common source line formed from the common region of the plurality of memory cells; and

a conductive bit line connected to the drain of each memory cell of the row.

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73. (Amended) A stacked gate region of a nonvolatile memory cell having a NOR structure comprising:

a field oxide region deposited in at least one sloped trench formed in a substrate, said at least one sloped trench having a base and an opening wider than said base;

a tunnel oxide layer formed on the substrate adjacent the field oxide region;

at least one floating gate layer formed over said tunnel oxide layer; and

at least one polysilicon structure formed adjacent to said at least one floating gate layer, said polysilicon structure is adapted to increase capacitive coupling of said memory cell.

74. The stacked gate region of claim 73 wherein said polysilicon structure is selected from the group consisting of at least one wing and at least one ear.

76. The stacked gate region of claim 74 wherein said polysilicon structure is at least one ear, said ear being formed adjacent to said field oxide region.

REMARKS

Claims 1-11, 13-18, 23, 26-32, 35, 39, 41-72, 75, and 77-90 are cancelled. Claims 12, 19-22, 24, 25, 33, 34, 36-38, 40, and 73 are amended. Therefore, claims 12, 19-22, 24, 25, 33, 34, 36-38, 40, 73, 74, and 76 are pending in this application.